Novel Field Effect Transistors for Low Power Electronics

Progress Report # 2

NAVY STTR Phase I
Contract Number: N00014-94-C-0260

November 28, 1994

Delivered To:

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From:

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Wm C.B. Peat 11/29/94
Dr. William C.B. Peatman, President

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November 29, 1994

Dr. Alvin M. Goodman
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Dear Dr. Goodman:

Please find enclosed Project Report #2 entitled "Novel Field Effect Transistors for Low Power Electronics" summarizing the status of our research under ONR STTR Contract #N00014-94-C-0260. Also enclosed is invoice #SA2-112894. If you should have any questions regarding either the report or the invoice, please don't hesitate to call me at the number above.

Thank you for your interest and support of Advanced Device Technologies, Inc.

Sincerely,

Wm C.B. Peatman

William C.B. Peatman
President

Attachments: Invoice #SA2-112894
Progress Report #2
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7. PAGE: 1 OF 1
8. ACCEPTANCE POINT: D

2. SHIPMENT NO.: ADT0002
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4. B/L TCN:
5. DISCOUNT TERMS: Net

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Original Invoice

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Approved for public release; distribution is unlimited.

Novel Field Effect Transistors for Low Power Electronics
(ONR STTR Contract N00014-94-C-0260)

Table of Contents

I. Phase I Technical Objectives

The primary objective of this Phase I project is to determine the extent of the significant reduction in power consumption of integrated circuits which may be achieved by utilizing a novel sidegate FET technology. The new FET technology promises to eliminate the Narrow Channel Effect (NCE) which is one of the primary factors limiting the minimum power consumption of integrated circuits. By eliminating the NCE, we will be able to scale the device size dramatically and reduce the power consumption by an order of magnitude. The project will assess the power, speed, circuit design, processing, and manufacturability of the new FET technology for both digital and analog circuit applications. In particular, we will extract device parameters from the new ultra-low power FETs fabricated at UVa, develop device models, incorporate these models into a new SPICE package (AIM-Spice), simulate different logic families including DCFL and SCFL, and compare the predicted performance with the standard DCFL and SCFL logic. We will also analyze the gate current leakage and subthreshold slope as the primary factors limiting the noise margins at low power supplies, establish the minimum required bias voltage for reliable operation, and analyze the factors determining the threshold voltage changes from device to device as well as other factors which may limit the yield and integration scale.

II. Phase I Progress Report #2

As detailed in the Phase I proposal, the project has five major tasks. These are 1) 2-D MESFET (discrete) device fabrication, 2) detailed device evaluation and optimization for next iteration of device design and fabrication, 3) parameter extraction using AIM-SPICE to generate and refine AIM-SPICE 2-D MESFET models, 4) 2-D MESFET DCFL and SCFL logic circuit simulations using AIM-SPICE and comparison with conventional circuits, and 5) analysis of manufacturability and technology insertion issues. This report summarizes the progress in each task area since the first Progress Report of 10/28/94.

Task 1: Device Fabrication

The critical dimensions of the 2-D MESFET include the channel width, W_0 and length, L_g and the drain-source spacing L_{DS}. Presently, there are two batches of 2-D MESFETs in progress having channel dimensions ranging from 0.5 - 1.0 micron (width) and 0.5 - 1.0 micron (length). These devices will provide new data for parameter extraction and device modeling.

One significant change in the fabrication will be tested in these new batches. Although earlier batches had a leakage (OFF) current of only 1 nA, even lower leakage currents may be possible using a lower damage gate etch process. Thus, a new SiCl4:BCl3 dry etch process is being evaluated as an alternative to the Cl2 chemically-assisted ion beam etch (CAIBE) which is suspected to cause excess damage (due to the 500 V Ar ion beam).

Task 2: Evaluation, Optimization, Design

The dc I-V characteristics of 2-D MESFET devices are being measured and cataloged in library files according to device dimensions and material parameters. Such cataloging is useful in developing a new 2-D MESFET device model. To date, both enhancement and depletion mode devices have been obtained. Recently, we measured a depletion mode device having the highest unit width current density and transconductance yet achieved in a 1.0 micron wide FET. The peak current density was 367 mA/mm and the peak transconductance was 295 mS/mm, both measured at V_{DS}=1.0V. Parameter extraction of this data is now underway using AIMSPICE[1] universal HFET model.

We have also begun evaluating the inverter operation using 2-D MESFETs for both the switching (input) transistor and the load, as illustrated in Fig. 1 (left). Both devices had nominal threshold voltages of 0V. The inverter transfer characteristic is shown in Fig. 1 (right). This characteristic is notable for the sharp transition between ON and OFF states. The voltage gain for this single inverter is $\Delta V_{out}/\Delta V_{in} = 9$. The inverter threshold voltage is comparable to that of the input FET. Higher threshold voltages will be obtained using enhancement mode FETs with higher V_T.

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1. AIM-SPICE was developed by Ytterdal, Fjeldly, Shur, and Lee and is available on INTERNET through anonymous FTP.

Task 3: 2-D MESFET AIM-SPICE Modeling

The measured transistor and inverter characteristics are accurately fitted using the universal HFET model of AIM-SPICE. So far, the HFET model yields a good agreement to the measured data, indicating that the so-called narrow channel effect is essentially eliminated in the 2-D MESFET.

Task 4: 2-D MESFET DCFL and SCFL Circuit Simulation

The device models for the 2-D MESFETs used in the inverter measurement were used to simulate the transfer characteristic shown in Fig. 1 (right). An excellent agreement between the inverter simulation and measurement were obtained. We are presently simulating loaded inverters (i.e. inverter chains, inverter driving multiple inverters, etc.) in order to better understand the 2-D MESFET circuit operation.

A major goal of this Phase I research is to evaluate the power-delay product of the 2-D MESFET. The power delay-product will be evaluated using AIMSPICE models which include capacitance of the 2-D MESFET. Such simulations will be useful to determine the application/market niche of the 2-D MESFET technology.

Task 5: Manufacturability and Technology Insertion Issues

A comprehensive technology analysis of 2-D MESFET circuits will be performed toward the end of Phase I project. It will serve to summarize the main advantages of the 2-D MESFET over existing technologies and to address any potential barriers to insertion of the 2-D MESFET technology into the large scale IC manufacturing environment.

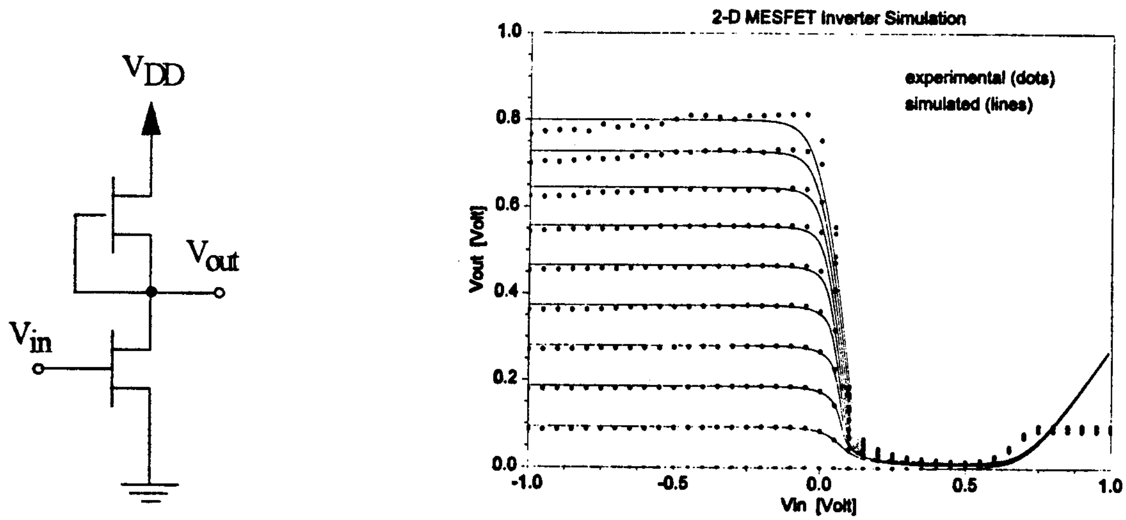

Fig. 1.Diagram of 2-D MESFET (DCFL) inverter (left) and transfer characteristics (right). The values of V_{DD} (above right) ranged from 0.9 V to 0.0V in -0.1V steps.

Distribution List

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